REMARKS/AGRUMENTS

Reconsideration of this application is respectfully requested. No new matter has been added.

Claim Rejections – 35 U.S.C. 102 and 35 U.S.C. 103

Claims **1-13, 15-30, and 32-32** stand rejected under 35 U.S.C. 102 as allegedly being anticipated by Nation et al. (US patent no. 6,233,599). Claim **36** stands rejected as allegedly being unpatentable over Nation in view of the official notice taken by the Examiner. The Applicants respectfully traverse the above-noted rejections for the reasons set out below, and request reconsideration of these rejections.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1

Claim 1 has been amended to clarify the limitations present in the original claim 1. Nation does not disclose "a method including maintaining a state machine to provide a multi-bit output, each bit of the multi-bit output indicating a respective status of an associated thread of multiple threads being executed with a multithreaded processor; detecting a change of status for a first thread within the multithreaded processor; and responsive to the change of status for the first thread within the multithreaded processor, configuring a functional unit within the multithreaded processor in accordance with the multi-bit output of the state machine" as required by claim 1.

Nation discloses saving the state of the active thread i, transferring the activity specified data for thread i from the activity specified register to the active register subset, and setting a corresponding flag within the thread status register (Nation 13:32-42), which is distinct from "configuring a functional unit". On the contrary, in Nation, while several operations are

performed on a thread responsive to a thread switch event (Nation 13:32-42), the thread controller maintains the same configuration. For example, processor registers are partitioned into a plurality of register subsets to enable the processor to execute a plurality of threads (Nation 7:35-45).

There is no indication that a functional unit in Nation is configured *responsive to the change of status for the first thread within the multithreaded processor*. On the contrary, Nation discloses using "a compiler capable of decomposing the task into threads, generation machine code for the threads and assigning a number of physical registers to each of the threads" (Nation 15:49-53). Thus, Nation discloses partitioning the resources when a task is first decomposed into a number of threads, which is in stark contrast to configuring a functional unit within the multithreaded processor *responsive to the change of status for the first thread within the multithreaded processor* as required by claim 1.

Although Nation discloses that the number of registers making up each register subset may be dynamically varied (Nation 8:1-3), there is no indication that dynamic partitioning occurs *responsive to the change of status for the first thread within the multithreaded processor*, or in accordance with the *multi-bit output* of the state machine, where *each bit of the multi-bit output indicating a respective status of an associated thread* of multiple threads being executed within a multithreaded processor as required by claim 1.

Because not every element of claim 1 is disclosed in Nation, claim 1 is patentable in view of Nation and should be allowed.

Claim 2.

Nation fails to disclose maintaining a state machine to provide a multi-bit output, wherein each bit of the multi-bit output indicates the status of the associated thread as being active or inactive as required by claim 2. The Office Action asserted that a READY flag in Nation corresponds to the "active" status of claim 2 and that "NOT-READY" flag corresponds to the "inactive" status of claim 2. The Examiner's attention is directed to Figure 5, where Nation discloses marking all loaded threads as "READY" at block 502, and then setting the active thread

as thread 0. Nation discloses a paradigm where a thread may have a status as "READY" but is not "active" (Nation 12:37-57), and thus a "READY" status does not correspond to an "active" status of claim 2.

Furthermore, claim 2 depends from an allowable claim 1 and thus is patentable.

Claims 3-17 are allowable for at least the reason of being dependent on claim 1.

Claim 18

Nation does not disclose an "apparatus comprising a state machine to provide a multi-bit output, each bit of the multi-output indicating a respective status of an associated thread of multiple threads being executed within a multithreaded processor, and to detect a change of status for a first thread within the multithreaded processor; and configuration logic to configure a functional unit within the multithreaded processor in accordance with the multi-bit output of the state machine" as required by claim 18.

Nation discloses using "a compiler capable of decomposing the task into threads, generating machine code for the threads and assigning a number of physical registers to each of the threads" (Nation 15:49-53). Nation further discloses that the number of registers making up each register subset may be dynamically varied (Nation 8:1-3). However, there is no indication that dynamic partitioning occurs in accordance with the *multi-bit output* of the state machine, where *each bit of the multi-bit output indicating a respective status of an associated thread* of multiple threads being executed with a multithreaded processor as required by claim 18.

Because not every element of claim 18 is disclosed in Nation, claim 18 is patentable in view of Nation and should be allowed.

Claims 35 and 36 are allowable for at least the reasons articulated with respect to claim 18.

If there are any deficiencies of fees associated with this communication, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

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